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TITLE

METHOD OF REDUCING TRENCH ASPECT RATIO

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor manufacturing process, and more particularly, to a method of reducing the aspect ratio of a trench.

Description of the Related Art

Semiconductor device geometry continues to decrease in size, providing more devices per fabricated wafer. Currently, some devices are fabricated with less than 0.25μm spacing between features; in some cases there is as little as 0.18μm spacing between features, which often takes the form of a trench.

An isolation technique called shallow trench isolation (STI) has been introduced to the fabrication of devices to reduce size. Isolation trenches are formed in a substrate between features, such as transistors. Figs. 1A~1B are schematic views of a traditional STI process.

In Fig. 1A, a substrate 10 such as a silicon wafer is provided. A shield layer 11 comprising a pad oxide layer 12 and a silicon nitride layer 14 is formed on part of the substrate 10. The shield layer 11 serves as a stacked mask defining an isolation area in the substrate 10. The pad oxide layer 12 can be a SiO_2 layer with a thickness of 50~150Å, formed by chemical vapor deposition (CVD) or thermal oxidation. The silicon nitride layer 14 can be a Si_3N_4 layer with a thickness of 800~1500Å, formed by CVD.

In Fig. 1B, using the shield layer 11 as a mask, part of the substrate 10 is etched to form a trench 15. A thin oxide film 16, serving as a linear layer, is then formed by thermal oxidation, conformal to the surface of the trench 15. The thickness of the thin oxide film 16 is about 180~220Å. Next, a trench-filling material such as a SiO_2 layer 18 is deposited in the trench 15 once with a conventional high-density plasma chemical vapor deposition (HDP-CVD). Typically, the HDP-CVD reaction gas includes O_2 and silane (SiH_4).

Fig. 1C shows that a void may form when a trench with a narrow gap is filled by a conventional process. For example, when the width of the trench 15 is less than 0.15μm and/or the aspect ratio of the trench is greater than 4, a void 20 is easily formed in a SiO_2 layer 19 with the conventional process. Such a void 20 seriously affects device reliability and yield, and hinders reduction in semiconductor device geometry.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a method of forming a shallow trench isolation (STI) in a substrate.

Another object of the present invention is to provide a method for lowering the aspect ratio of a trench during a deposition process to fill the trench without creating voids.

In order to achieve these objects, the present invention provides a method of reducing the aspect ratio of a trench. A trench is formed in a substrate. Using HDP-CVD, a conformal first oxide layer is formed on a surface of the trench. A conformal first nitride layer is formed on the first oxide layer. A portion of the first nitride layer is removed to cause the first

nitride layer to be lower than a top surface of the substrate. Using a BOE solution, the first nitride layer and a portion of the first oxide layer are removed and thus leave a remaining first oxide layer on a lower portion of the surface of the trench.

Moreover, when the aspect ratio of the trench is high, subsequent to the above steps, at least one cycle of the following steps can be performed. Using HDP-CVD, a conformal second oxide layer is formed on the remaining first oxide layer and the surface of the trench. A conformal second nitride layer is formed on the second oxide layer. A portion of the second nitride layer is removed, thereby causing the second nitride layer to be lower than a top surface of the substrate. Using a BOE solution, the second nitride layer and a portion of the second oxide layer are removed and thus produce a remaining second oxide layer on the remaining first oxide layer. Thus, the aspect ratio can be further reduced.

The present invention improves on the related art in that the present method leaves an oxide layer on the lower surface of the trench and thus produces a dual "U" shaped trench rather than the conventional single "U" shaped trench. Thus, the invention can reduce the aspect ratio of the trench, thereby preventing void formation during trench filling and ameliorating the disadvantages of the related art.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein:

Figs. 1A~1B are sectional views according to the conventional STI process;

Fig. 1C is a schematic view, according to the conventional STI process, that forms a void in a trench; and

Figs. 2~12 are sectional views according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the invention will now be described in detail with reference to the accompanying drawings. Figs. 2~12 are sectional views showing the trench isolation process of the present invention.

In Fig. 2, a semiconductor substrate 200, such as a silicon wafer, is provided. A shield layer 205 preferably comprising a pad oxide layer 210 and a silicon nitride layer 220 is formed on part of the substrate 200. The pad oxide layer 210 can be a SiO_2 layer formed by thermal oxidation or CVD (chemical vapor deposition). The silicon nitride layer 220 can be a Si_3N_4 layer formed by CVD. For example, the thickness of the pad oxide layer 210 is about 100Å and the thickness of the silicon nitride layer 220 is about 900Å. The shield layer 205 serves as a stacked mask for defining an isolation area in the substrate 200.

In Fig. 3, using the shield layer 205 as a mask, part of the substrate 200 is etched to form a trench 310. The depth of the trench 310 is, for example, 2600~5000Å. Moreover, a thin oxide film (not shown), such as a SiO_2 film, can be conformably formed on the side and the bottom of the trench 310 by thermal oxidation. The thin oxide film (not shown) of about 180~220Å in thickness serves as a linear layer. In order to simplify the

illustration, the thin oxide film (or the linear layer) is not shown in Figs.2~12.

In Fig. 4, using HDP-CVD, a conformal first oxide layer 410, such as a SiO_2 layer, is formed on the surface of the trench 310. The thickness of the first oxide layer 410 is about 200~300Å. It is noted that, because of HDP-CVD, the structure of the first oxide layer 410 is adequately dense. The conditions of the HDP-CVD comprise, for example, the process gas using SiH_4 and O_2 and as ratio of SiH_4/O_2 with about 1.5~2, an operational temperature of about 550~650°C and an operational pressure of about 5m torr.

In Fig. 4, a conformal first nitride layer 420, such as a Si_3N_4 layer, is formed on the first oxide layer 410 by, for example, low pressure chemical vapor deposition (LP-CVD). The thickness of the first nitride layer 420 is about 40~50Å.

In Figs. 5 and 6, the trench 310 is filled with a photoresist layer 510. The photoresist layer 510 is then partially etched back to form a first photoresist layer 510' (i.e. a remaining photoresist layer 510') in the trench 310 and covers part of the first nitride layer 420. It is noted that the first photoresist layer 510' is at least 1000Å lower than a top surface of the substrate 200. The symbol "d" shown in Fig. 6 indicates the distance (at least 1000Å) between the first photoresist layer 510' and the top surface of the substrate 200.

In Fig. 7, using the first photoresist layer 510' as a mask, the exposed portion of the first nitride layer 420 is removed to leave a remaining first nitride layer 420'. Similarly, the remaining first nitride layer 420' is at least 1000Å lower than the top surface of the substrate 200.

In Fig. 8, the first photoresist layer 510' is then removed.

In Fig. 9, using a BOE (buffer oxide etcher) solution, the first nitride layer 420' and part of the first oxide layer 410 are removed to leave a remaining first oxide layer 410' on the lower surface of the trench 310.

As an operational example, the etching procedure uses a BOE solution consisting of NH_4F(40%), HF(49%) and deionized water (DI). The volume ratio of NH_4F/HF/DI is about 5/1/48. In this example, the etching rate of the first oxide layer 410 with the BOE solution is about 280~320Å/min and the etching rate of the remaining first nitride layer 420' is about 8~12Å/min. When the remaining first nitride layer 420' is thoroughly removed, the etching procedure halts. The remaining first oxide layer 410' is thus left on the lower surface of the trench 310, thereby reducing the aspect ratio of the trench 310.

Here, a demonstration of the present invention is provided, illustrating the reduced trench aspect ratio. Subsequent to the present process, referring to Fig. 9, it is assumed that: p=1000Å, w=800Å, x1=200Å, x2=400Å, h1=2650Å, h2=2900Å, h3=250Å, h4=2000Å.

The original aspect ratio (AR)

= (h2+p)/w = 3900/800

= 4.87

Subsequent to the present process, the aspect ratio (AR')

= AR*[(h1-h4)*x2+(h4+p)*w/(h2+p)*w]/[(h2+p)*w]

= 4.87*[(650*400+3000*800)/(3900*800)]

= 4.87*0.85

= 4.14

Moreover, when the aspect ratio of the trench is very high, at least one cycle of the following steps, similar to Figs. 4~9, can be performed to further reduce the aspect ratio.

Similar to Fig. 4, using HDP-CVD, a conformal second oxide layer (not shown) is formed on the remaining first oxide layer 410' and the surface of the trench 310.

Similar to Fig. 4, using LP-CVD, a conformal second nitride layer (not shown) is formed on the second oxide layer (not shown).

Similar to Figs. 5 and 6, a photoresist recess procedure is performed. That is, a second photoresist layer (not shown) is formed in part of the trench 310 to cover part of the second nitride layer (not shown). The second photoresist layer (not shown) is at least 1000Å lower than the top surface of the substrate 200.

Similar to Fig. 7, using the second photoresist layer (not shown) as a mask, part of the second nitride layer (not shown) is then removed.

Similar to Fig. 8, the second photoresist layer (not shown) is removed.

Similar to Fig. 9, using the BOE solution, the second nitride layer (not shown) and part of the second oxide layer (not shown) are removed to leave a remaining second oxide layer (not shown) on the remaining first oxide layer 410'. Consequently, the aspect ratio of the trench 310 can be further reduced.

Next, referring to Fig. 10, using HDP-CVD or TEOS-CVD, the trench 310 is filled with an insulation layer 1010 extending onto the shield layer 205. The insulation layer 1010 is, for example, a SiO_2 layer. Due to the lower aspect ratio of the trench 310

according to the present method, void-free deposition is easily achieved.

In Fig. 11, a planarization such as chemical mechanical polishing (CMP) is performed on the insulation layer 1010 to produce a smooth insulation layer 1010', wherein the shield layer 205 serves as a stop layer for the planarization.

In Fig. 12, the silicon nitride layer 220 is removed by, for example, a phosphoric acid solution. The pad oxide layer 210 is removed by, for example, an HF solution. Thus, a void-free STI profile 1210 is formed.

Thus, the present invention provides a method of forming a void-free STI in a substrate, and a method of lowering the aspect ratio of a trench during a deposition process of filling the trench. Additionally, the present invention significantly improves the reliability of the product and achieves the goal of reduction in IC size.

Finally, while the invention has been described by way of example and in terms of the above, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.